New developments of an LLRF control system for superconducting cavities at IPNO

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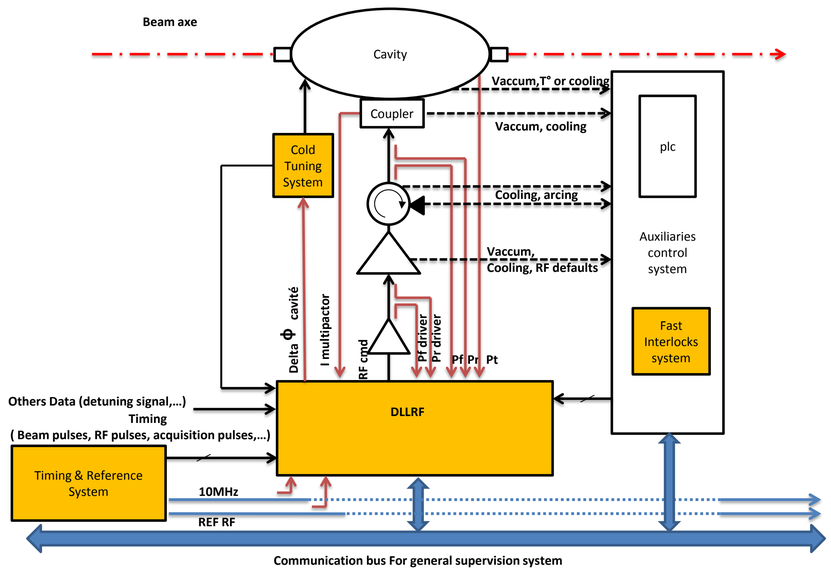
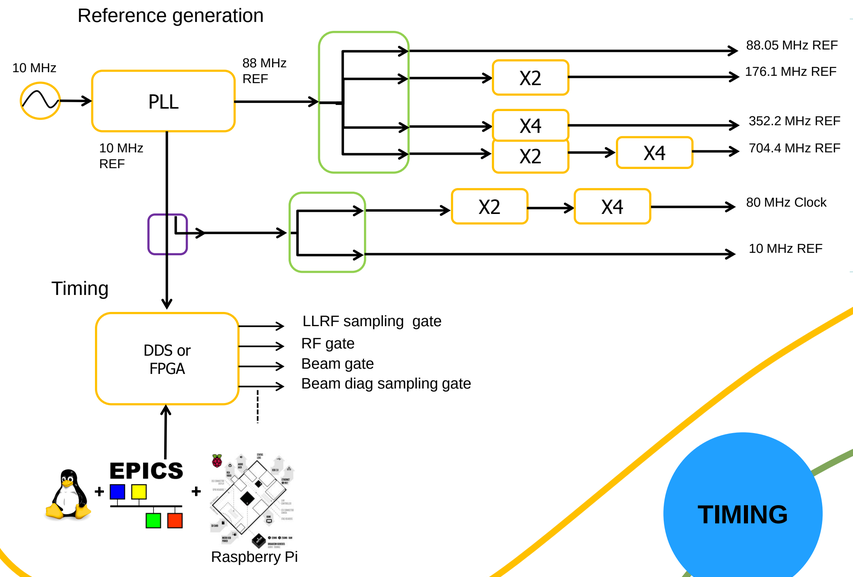
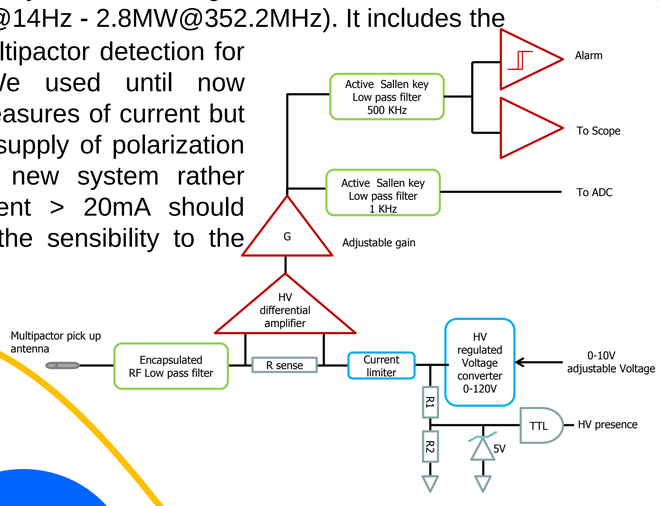


Within the framework of the current research programs on High Intensity Proton Accelerators, a first collaboration with the CNRS/LPNHE Lab has given one PXI's version of a Low Level Radio Frequency Digital system used for our R&D on superconducting cavities. Today a new development of an LLRF digital system is in progress at IPN Orsay, around an in-house mother board with a FPGA and an ARM processor with a LINUX OS and EPICS IOC. All sub-systems needed for operating on accelerator are also in progress in the framework of several projects at IPNO, as the Cold Tuning System digital controller developed with ADEX© (MAX project), the analogue Self Exciting Loop for RFQ (MYRRHA project) and the interlock system including multipactor detection and measurements (SPARE project). Our goals are also to use atypical technologies as ETHERNET for the communication and supply link (PoE) for example. This poster focuses on the global developments: details of each sub-system with the associated project, the main options which will be implemented and the schedule.

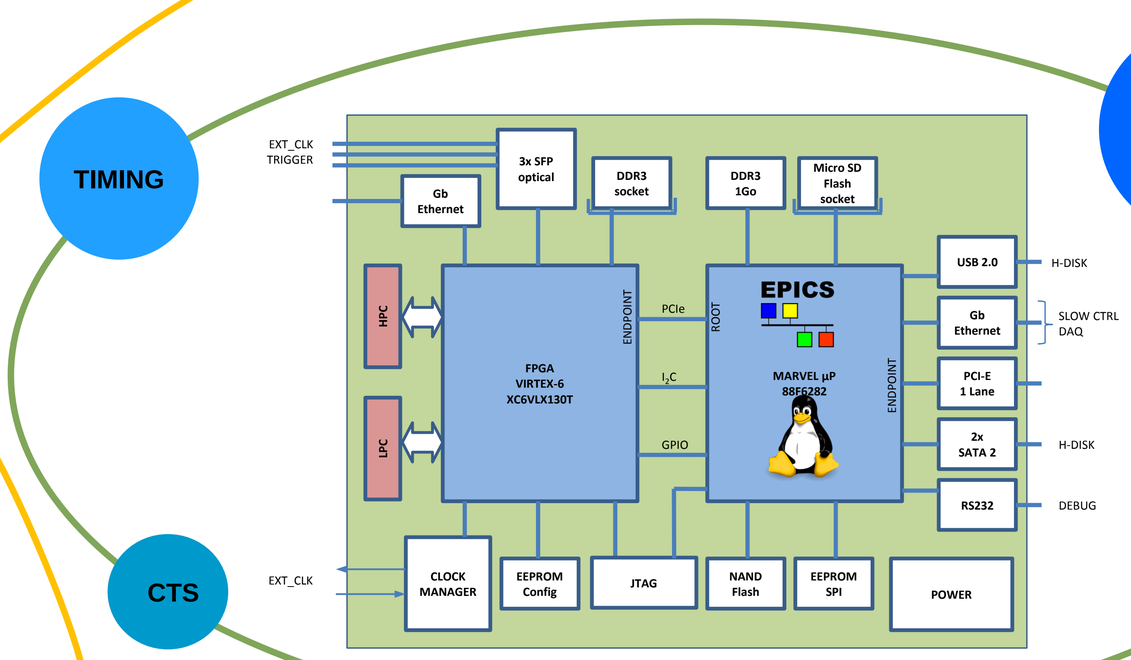
Within the framework of our R&D, this prototype system integrates the generation of reference frequencies (jitter of +/-0.1°), a mechanism of timing and a regulation of temperature. With a Module using a processor ARM, it should later become a plug and play system EPICS.



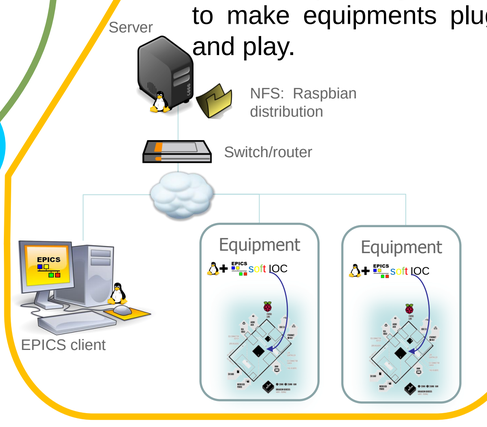
A system of fast interlock is necessary for the management of the next station of RF pulsed power (1.5ms@50Hz or 3ms@14Hz - 2.8MW@352.2MHz). It includes the development of an electronics of multipactor detection for testing cavities with couplers. We used until now converters I/V adapted to the low measures of current but strongly subject to the noise of the supply of polarization involving the use of battery. This new system rather adapted to the measures of current > 20mA should nevertheless agree and to reduce the sensibility to the noise of the supply.

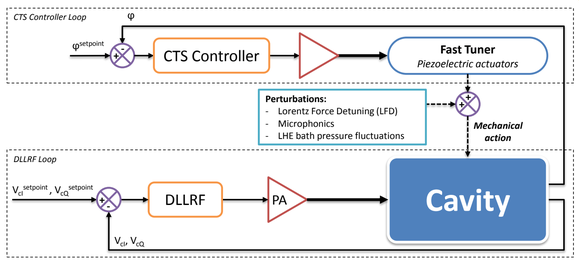


Digital core

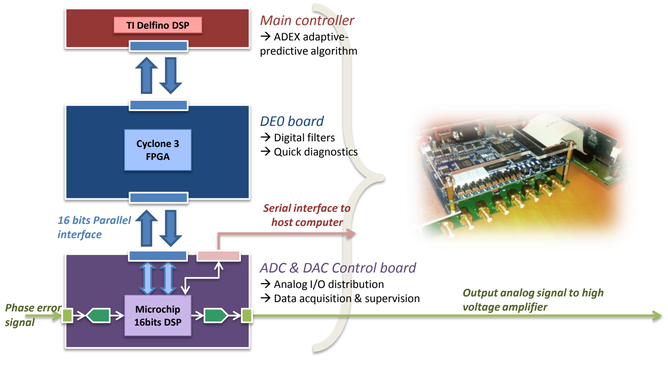


Through Raspberry Pi, the tests of validation of our configuration are in progress. The purpose is to obtain a feasible OS via NFS incorporating a IOC to make equipments plug and play.





The standard tool generally used to control process variables is PID. This technology has its limitations and usually needs manual adjustment which can be tedious and requires experiment through trial and error. Here the idea is to optimize the control process thanks to an adaptive-predictive algorithm developed by ADEX.



Theory of operation:

1- An ADC & DAC control board acquires the phase error signal of the cavity

2- Information is sent from a dsPIC to the DE0 board for digital filtering and returns the result to the main controller

3- Main controller (Delfino) receives and processes the digital filtered signal and returns the output signal to the DACs of the Control board via the DE0 board.

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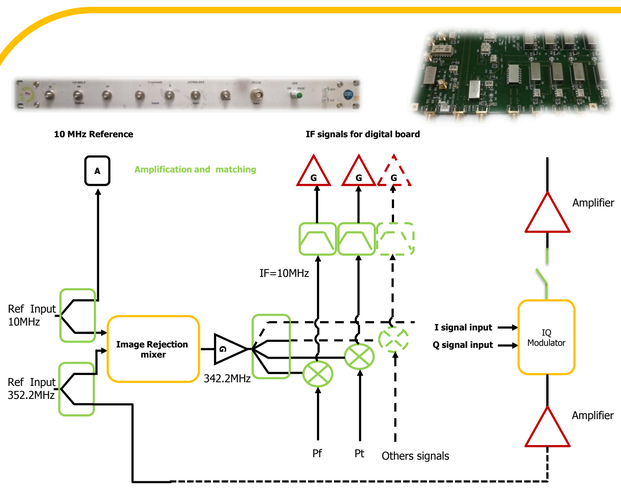

Characteristics	
Frequency	352MHz
Bandwidth	40 MHz
Attenuator	63.5 dB by 0.25dB step, low phase variations
Phase Shifter	360° by 1° step
Limiting Amplifier	60 dB of range , low phase variations
Max Output level	4.5 dBm

The down converter system, necessary for the digitalization of the RF signals is added to RF switch as well as a modulator IQ, used as actuator for the regulation. The Self Exciting Loop was recently validated on PCB with the optional implementation of an actuator. The following stage will consist in associating them to obtain according to the need an analog or digital system, with or without S.E.L. This systems can be realized with frequencies between 88 MHz and 352MHz easily.

All the presented systems is in progress (test or realization) within the framework of various projects of the laboratory. Our objective is to obtain in 2014 a first operational version of all these systems allowing us to comprehend the major part of the associated themes, to compare solutions for multipactor detection , power supply etc…